In the Claims:

A complete listing of the pending claims with proper claim identifiers is set forth below.

1. (Previously presented) A packet processing system comprising:

a processor;

a co-processor separated from said processor by a boundary; and

an interface coupled with said processor and said co-processor and operative to bridge said boundary, said interface including:

a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and

control logic coupled with said at least two read/write ports;

wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor;

said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and

said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and

wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously.

2. (Original) The packet processing system of Claim 1, wherein said boundary comprises a printed circuit board-to-printed circuit board connector coupled between said processor and said co-processor.

3. (Previously presented) The packet processing system of Claim 1, wherein said processor communicates with a first protocol and said co-processor communicates with a second protocol, said boundary comprising a difference between said first and second protocols, said interface being further operative to translate data between said first and second protocols.

4. (Original) The packet processing system of Claim 1, wherein said processor is a network processor.

5. (Original) The packet processing system of Claim 1, wherein said co-processor is a task specific processor.

6. (Original) The packet processing system of Claim 5, wherein said co-processor is a content addressable memory.

7. (Original) The packet processing system of Claim 5, wherein said co-processor is a classification processor.

8. (Original) The packet processing system of Claim 1, wherein said control logic signals said processor when said co-processor has stored data to said memory.

9. (Original) The packet processing system of Claim 1, wherein said control logic signals said co-processor when said processor has written data to said memory.

10. (Original) The packet processing system of claim 1, wherein said memory comprises a dual ported sync-burst static random access memory.

11. (Previously presented) An interface for coupling a processor to a co-processor across a boundary, said processor and said co-processor being separated by said boundary, said interface comprising:

a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and

control logic coupled with said at least two read/write ports;

wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor;

said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and

said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and

wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously.

12. (Original) The interface of Claim 11, wherein said boundary comprises a printed circuit board-to-printed circuit board connector coupled between said processor and said co-processor.

13. (Original) The interface of Claim 11, wherein said processor communicates with a first protocol and said co-processor communicates with a second protocol, said boundary comprising a difference between said first and second protocols.

14. (Original) The interface of Claim 11, wherein said processor is a network processor.

15. (Original) The interface of Claim 11, wherein said co-processor is a task specific processor.

16. (Original) The interface of Claim 15, wherein said co-processor is a content addressable memory.

17. (Original) The interface of Claim 15, wherein said co-processor is a classification processor.

18. (Original) The interface of Claim 11, wherein said control logic signals said processor when said co-processor has stored data to said memory.

19. (Original) The interface of Claim 11, wherein said control logic signals said co-processor when said processor has written data to said memory.

20. (Original) The interface of claim 11, wherein said memory comprises a dual ported sync-burst static random access memory.

21. (Original) The interface of claim 11, wherein said interface allows said processor to communicate with said co-processor as if said co-processor was directly connected with said processor.

22. (Original) The interface of claim 11, wherein said interface allows said processor to operate independently of the interface requirements of said co-processor.

23. (Original) The interface of claim 11, wherein said processor is located on a first circuit board and said co-processor is located on a second circuit board coupled with said first circuit board by a first connector, said first connector characterized by at least one electrical characteristic, said interface operative to isolate said processor and said co-processor from said at least one electrical characteristic.

24. (Previously presented) A method of interfacing a processor with a co-processor across a boundary, said processor and said co-processor being separated by said boundary, said method comprising:

(a) receiving first data from said processor via a first interface;

(b) storing said first data in a memory;

(c) signaling said co-processor that said first data has been stored;

(d) receiving a read command from said co-processor via a second interface; and

(e) providing said first data to said co-processor via said second interface across said boundary;

wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously.

25. (Original) The method of Claim 24, further comprising:

(f) receiving second data from said co-processor via said second interface;

(g) storing said second data in said memory;

(h) signaling said processor that said second data has been stored;

(i) receiving a read command from said processor via said first interface; and

(j) providing said second data to said processor via said first interface across said boundary.

26. (Original) The method of Claim 24, wherein said providing further comprises providing said first data across a boundary comprising a printed circuit board-to-printed circuit board connector.

27. (Original) The method of Claim 24, said method further comprising using a network processor as said processor.

28. (Original) The method of Claim 24, said method comprising using a task specific processor as said co-processor.

29. (Original) The method of Claim 28, wherein said co-processor is a content addressable memory.

30. (Original) The method of Claim 28, wherein said co-processor is a classification processor.

31. (Original) The method of Claim 24, wherein said signaling is performed by control logic signal coupled with said memory.

32. (Original) The method of claim 24, wherein said memory comprises a dual ported sync-burst static random access memory.

33. (Original) The method of claim 24, wherein said processor communicates with said co-processor as if said co-processor was directly connected with said processor.

34. (Previously presented) An apparatus for facilitating communications between a first processor and a second processor, the apparatus comprising:

a dual port memory coupled with said first processor via first interface and said second processors via a second interface, and operative to act as a message buffer between said first processor and said second processor; and

control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors of said communications;

wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously.

35. (Original) The apparatus of claim 34, wherein said first processor comprises a network processor.

36. (Original) The apparatus of claim 34, wherein said second processor comprises a task specific processor.

37. (Original) The apparatus of claim 36, wherein said second processor comprises a content addressable memory.

38. (Original) The apparatus of claim 36, wherein said second processor comprises a classification processor.

39. (Original) The apparatus of Claim 34, wherein said control logic signals said first processor when said second processor has written data to said dual ported memory and said control logic signals said second processor when said first processor has written data to said dual ported memory.

40. (Original) The apparatus of Claim 34, wherein said dual ported memory comprises a dual ported sync-burst static random access memory.

41. (Previously presented) The apparatus of Claim 34, wherein said first processor communicates with said second processor as if said second processor was directly connected with said first processor.